a semiconductor substrate;

an element isolation region formed in the semiconductor substrate, the element isolation region isolating a plurality of element regions in the semiconductor substrate;

a first transistor formed in a peripheral circuit portion of the semiconductor substrate, the first transistor including source and drain diffusion layers formed in one of the plurality of element regions and a gate electrode having a first gate length;

a second transistor formed in a memory cell portion of the semiconductor substrate, the second transistor including source and drain diffusion layers formed in another of the plurality of element regions and a gate electrode having a second gate length shorter than the first gate length;

A2 cont.

a contact connected to one of the source and drain diffusion layers; and

a first insulating film different from a silicon oxide covering the second transistor and not covering the first transistor, the first insulating film being an etching stopper for the contact to the element isolation region and having a property which makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide.

2. (Amended) The nonvolatile semiconductor memory device according to claim 1, wherein the gate electrode of the second transistor has a stacked gate structure which includes a floating gate formed on a gate insulating film, an inter-gate insulating film formed on the floating gate and a control gate including a metal or a metal compound containing silicon formed on the inter gate insulating film.

3. (Amended) The nonvolatile semiconductor memory device according to claim 1, further comprising:

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a second insulating film which is different from the first insulating film and formed between at least the gate electrode of the second transistor and the first insulating film.

11. (Amended) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a plurality of erasable and programmable memory cell transistors;

a plurality of peripheral transistors comprising peripheral circuits;

an insulating film covering a side and a top of both the plurality of erasable and programmable memory cell transistors and the plurality of peripheral transistors, the

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insulating film comprised primarily of silicon and nitrogen, and a surface of the insulating film being oxidized.

12. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the insulating film has a thickness of at most 50 nm.

13. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the thickness of an oxidized region of the insulating film is not smaller than 1 nm and not larger than 10 nm.

14. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the concentration of hydrogen in the insulating film is not larger than $3 \times 10^{21}$ atom/cm$^3$.

**Please add new Claims 19-25 as follows:**

19. (New) The nonvolatile semiconductor memory device according to claim 11, further comprising:

a semiconductor substrate;

an element isolation region formed in the semiconductor substrate, the element isolation region isolating a plurality of element regions in the semiconductor substrate;

a diffusion layer formed in one of the plurality of element regions; and

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a contact connected to the diffusion layer,

wherein the insulating film has a part formed on the element isolation region and the insulating film is an etching stopper for the contact to the element isolation region.

20. (New) The nonvolatile semiconductor memory device according to claim 11, wherein the insulating film has a concentration gradient in which the hydrogen concentration gradually becomes higher near a surface of the insulating film.

21. (New) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

an element isolation region in the semiconductor substrate, the element isolation region isolating a plurality of element regions in the semiconductor substrate;

a plurality of erasable and programmable memory cell transistors each having source and drain diffusion layers in one of the plurality of element regions;

a plurality of peripheral transistors each having source and drain diffusion layers in another of the plurality of element regions, the plurality of peripheral transistors comprising a peripheral circuit;

a contact connected to one of the source and drain diffusion layers; and

an etching stopper insulating film, for the contact to the element isolation region, formed on the element isolation region and the plurality of memory cell transistors, the etching stopper comprised primarily of silicon and nitrogen, and a surface of the etching stopper insulating film being oxidized.

22. (New) The nonvolatile semiconductor memory device according to claim 21, wherein the etching stopper insulating film has a concentration gradient in which the hydrogen concentration gradually becomes higher near a surface of the etching stopper insulating film.

23. (New) The nonvolatile semiconductor memory device according to claim 21, wherein the etching stopper insulating film has a thickness of at most 50 nm.

24. (New) The nonvolatile semiconductor memory device according to claim 21, wherein the thickness of an oxidized region of the etching stopper insulating film is not smaller than 1 nm and not larger than 10 nm.

25. (New) The nonvolatile semiconductor memory device according to claim 21, wherein the concentration of hydrogen in the etching stopper insulating film is not larger than $3 \times 10^{21}$ atom/cm$^3$.

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IN THE ABSTRACT

**Please delete the paragraph at page 38, lines 2-13, in its entirety and substitute**